Implementation of Parity Logic

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EECS: 1100 Digital Logic Design
The University of Toledo

Lab Assignment #4

1. Objectives

- getting familiar with parity function,
- introduction to error detection using parity codes,
- gaining experience in creating logic circuit representation of logic functions,
- developing skills in analyzing and testing the behavior of combinational logic circuits.

2. Prelab Assignment

2.1 EVEN AND ODD PARITY FUNCTION

2.1.1 Show as equations (2.1-1) and (2.1-2) the expressions of three-variable even and odd parity functions P_e (a,b,c) and P_o (a,b,c). Show as equations (2.1-3) and (2.1-4) the expressions of four-variable even and odd parity functions P_e (a,b,c,d) and P_o (a,b,c,d).

2.1.2 Prepare two truth tables,

- table T2.1-1 of the even and odd parity functions P_e3 (a,b,c) and P_o 3 (a,b,c),
- table T2.1-2 of the even and odd parity functions P_e4 (a,b,c,d) and P_o 4 (a,b,c,d).

2.1.3 Suppose that some operation has a need of transferring a 3-bit encoded stream of data through a noisy transmission channel between locations A and B. Further suppose that the correct functioning of this information transfer ought to be monitored by a single-bit error detection code. For the purpose of implementing the required error detection in the transmission channel, design:

(a) a logic circuit of an even parity generator **(PG)** to be used for error-detection encoding at location A; show a drawing of the designed logic circuit as Figure 2.1-1(a)

(b) a logic circuit of a parity checker **(PC)** for single bit errors to be used at location B; show a drawing of the designed logic circuit as Figure 2.1-2(a).

2.1.4 Using integrated circuit components listed in section 3.2, design a physical layout of the logic circuits shown in Figure 2.1-1(a) and 2.1-2(a). Show the computer generated drawings of the designed layouts as Figures 2.1-1(b) and 2.1-2(b) respectively. Provide IC package pinouts in all drawings of Figures 2.1-1 and 2.1-2.

Hint#1 Pinouts (pin numbers) are available in Figure 2.5 of the course text book, pp.107-109, and in the TTL Data Book.

3. Lab Equipment and Circuit Components

3.1 EQUIPMENT

Equipment to be used includes:

- Proto boards: Global PB-104, or PB-105,
- Agilent E3631A DC power supply,
- Function generator: Agilent 33120A,
- Mixed-Signal oscilloscope Agilent 54645D,
- Dell GxaEM computer system.

3.2 LOGIC GATE AND CIRCUIT COMPONENTS

- IC component 7404, hex inverter gate, (1)
- IC component 7486, quad 2-input EXOR gates, (2)
- IC component 7493, 4-bit ripple counter. (1)

4. Lab Experiment

4.1 EVEN AND ODD PARITY FUNCTION

4.1.1 Using the prepared physical circuit diagrams of Figure 2.1-1(a) and 2.1-1(b) as a reference, build on proto board an implementation of the parity generator and parity checker logic functions, which are shown in Figure A.4-1 as logic blocks PG and PC.

4.1.2 Add to the logic blocks PG and PC the remaining components which create the experimental circuit shown in figure A.4-1. Note that the Function generator and the IC 7493 act together as the *data stream source* at location A.

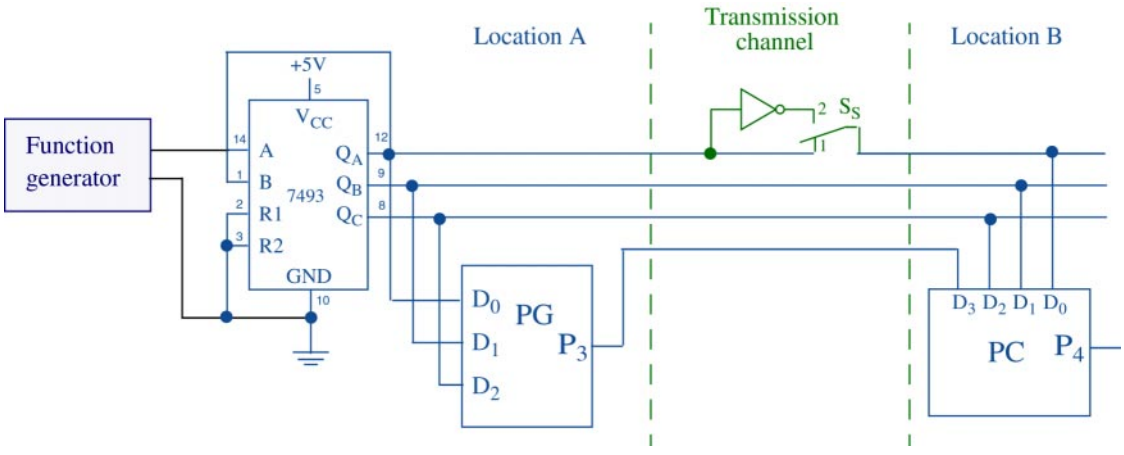

Figure A.4-1 Test circuit for the parity generator and parity checker circuits.

4.1.3 Connect digital channels D0 through D6 of the Agilent 54645D to the circuit constructed under A.4-1:

- digital channel D0 to input D 0 of the PG block,
- digital channel D1 to input D 0 of the PC block,

- digital channels D2 through D3 to *data stream source* lines Q_B through Q_C respectively,
- digital channel D4 to output P_3 of the PG block,
- digital channel D5 to output P_4 of the PC block,
- digital channel D6 to output of the function generator, Agilent 33120A

Establish a ground connection. Use a jumper wire to implement the switch SS in position 1. Turn on digital channels D0 through D6, and label them Q_A, S_S, Q_B, Q_C, P_3, P_4, and F_G respectively.

4.1.4 Adjust the frequency of the function generator to 1MHz. Set the triggering mode of the Agilent 54645D to combination 000 on channels D1 through D3. Hit the key Single on the Agilent 54645D. Adjust the display of waveforms so that the first appearance of the combination of signal values 000 on channels D1 through D3 is positioned at the left end of the screen, and that the whole screen shows ten percent more than just two periods of the signal at Q_C .

4.1.5 From the obtained waveforms, determine the truth tables of the circuit blocks PG and PC. Show the truth table of PG as table T4.1-1 and the truth table of PC as table T4.1-2.

4.1.6 Compare the truth table T4.1-1 of the circuit block PG to truth table of the P_3 (a,b,c), and compare the truth table T4.1-2 of the circuit block PC to truth table of the function P_4 (a,b,c,d). If they are equal proceed to Section 4.1.7; otherwise, first find the cause of the discrepancy and correct it.

4.1.7 Save the Screen Image of the waveforms of channels D0 through D5 to a file named L4_417.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.1.8 To simulate a single-bit error introduced by the signal transmission channel, reconnect the jumper wire to implement the switch SS in position 2; then capture on the oscilloscope's screen a new version of signal waveforms, the same way it was done in 4.1-4. Verify the correct functioning of the circuit block PC by checking its output P_4 against the truth table of the function P_4 (a,b,c,d) which was prepared in Section 2.1.2.

4.1.9 Save the Screen Image of the waveforms of channels D0 through D5 to a file named L4_419.tif on the Dell GxaEM computer system. (Alternatively, use the Screen Capture tool.)

4.2 TRANSFER OF CAPTURED WAVEFORMS.

Transfer (ftp) the files L4_*.tif from the Dell GxaEM computer system to your personal College of Engineering computer account.

5. Postlab Assignment

5.1 ANALYSIS OF EXPERIMENTAL RESULTS.

5.1.1 Using the waveforms captured as a result of the experiment performed in Section 4.1.4, make a conclusion as to which set of conditions at the inputs of the block PG cause the output of PG to have the value of logical one.

5.1.2 Using the waveforms captured as a result of the experiment performed in Sections 4.1.8, make a conclusion as to which set of conditions at the inputs of the block PC cause the output of PC to have the value of logical one.

6. Lab Report

To be considered complete, the Lab report must contain the following,

1. Cover sheet - Lab style, filled out,
2. The result of work under 2.1.
3. The result of work under 4.1.
4. A report on items not already included under 2. and 3. above, which includes:
   - a discussion of the insights gained through the conducted experiments,
   - textual description and graphical/ tabular illustration of the design procedure(s),
   - description of implemented testing procedures,
   - conclusions reached as a result of performing the lab experiment,
   - comments and suggestions that might lead to easier and/or deeper understanding of the topics covered by the assignment.